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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,960	03/10/2004	Chien-Hao Chen	67,200-1216	7718

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EXAMINER	
TRAN, MAI HUONG C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,960	CHEN ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) *31-43* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Applicant's election with traverse of Group II (claims) drawn to process of making a semiconductor device is acknowledged. Accordingly, claims 31-43 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Because Applicant did not distinctly and specifically point out the supposed error in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

The traversal is on the ground(s) that see the election paper. This is not found persuasive because the fields of search for method' and device claims are NOT coextensive and the determinations of patentability of method and device claims are different, that is process limitations and device limitations are given weight differently in determining the patentablitity of the claimed inventions. Also, the strategies for doing text searching of the device claims and method claims are different. Thus, separate searches are required.

The requirement is still deemed proper and is therefore made **FINAL**.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-30 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,890,808 to Chidambarrao et al.

Regarding to claim 1, Chidambarrao discloses a method for improving charge mobility in a MOSFET device comprising the steps of providing a first gate 18 with a first semiconductor conductive type and a second gate 20 with a second semiconductor conductive type overlying a substrate 1, 2, 3; forming a first strained layer with a first type of stress overlying said first gate; and forming a second strained layer with a second type of stress overlying said second gate (col. 2, lines 50-67, col. 3, lines 1-30, lines 52-59, col. 4, lines 18-27, and figs. 2a-2h).

Regarding to claim 2, the method further comprising the step of transferring the first stress type from the first strained layer to the first gate and the second stress type from the second strained layer to the second gate (col. 2, lines 50-67, col. 3, lines 1-30).

Regarding to claim 3, the method further comprising the step of removing the first and second strained layers (col. 2, lines 50-67, cols. 3-6).

Regarding to claim 4, the method wherein an oxide layer is formed over the first and second gates prior to the steps of forming a first and second strained layer (col. 2, lines 50-67, cols. 3-6).

Regarding to claim 5, the method wherein an ion implantation process to form dopant regions including forming an amorphous portion in the first and second gates prior to the steps of forming a first and second strained layer (col. 2, lines 50-67, cols. 3-6).

Regarding to claim 6, the method further comprising the step of carrying out an annealing process to recrystallize the amorphous portion following the steps of forming a first and second strained layer (cols. 2-6).

Regarding to claim 7, the method wherein the first and second stress types are selected from the group consisting of tensile stress and compressive stress formed over a respective N conductive type gate and P conductive type gate (col. 3, lines 22-30).

Regarding to claim 8, the method wherein the steps of forming a first and second strained layer comprise the steps of forming the first strained layer; removing a first portion of the first strained layer over one of the first and second gates to leave an uncovered portion; and forming the second strained layer over the uncovered portion (col. 2, lines 50-67, cols. 3-6).

Regarding to claim 9, the method wherein the first and second strained layers are deposited by a CVD process selected from the group consisting of LPCVD, ALCVD, and PECVD (cols. 3-4).

Regarding to claim 10, the method wherein the first and second strained layers comprise a nitride (cols. 2-6).

Regarding to claim 11, the method wherein the first and second strained layers are selected from the group consisting of silicon nitride and silicon oxynitride (col. 3, lines 63-66).

Regarding to claim 12, the method wherein the first and second strained layers comprise a stress level up to about 2 Gpa (col. 3, lines 19-21).

Regarding to claim 13, the method wherein the first and second strained layers are formed at a thickness from about 50 Angstroms to about 1000 Angstroms (col. 4, lines 41-45).

Regarding to claim 14, the method wherein the steps of forming the first and second strained layers is carried out at a temperature less than about 600 degrees Celsius (col. 5, lines 33-35).

Regarding to claim 15, Chidambarrao discloses a method for improving charge mobility in a MOSFET device comprising the steps of providing a first gate 18 with a first semiconductor conductive type and a second gate 20 with a second semiconductor conductive type overlying a substrate 1, 2, 3; forming a first strained layer with a first type of stress overlying said first gate; forming a second strained layer with a second type of stress overlying said second gate; transferring the first stress type from the first strained layer to the first gate and the second stress type from the second strained layer to the second gate; and removing the first and second strained layers (col. 2, lines 50-67, cols. 3-6, and figs. 2a-2h).

Regarding to claim 16, Chidambarrao discloses a method for improving charge mobility in a MOSFET device comprising the steps of providing a substrate comprising at least one polysilicon gate electrode; performing an ion implantation process to form dopant regions including forming an amorphous portion in the at least one polysilicon gate electrode; forming a first dielectric layer comprising a selected stress level selected from the group consisting of tensile stress and compressive stress over the at least one polysilicon gate electrode; and carrying out an annealing process to recrystallize the amorphous portions of the respective polysilicon gate electrodes to form a stress level in the substrate (cols. 2-6).

Regarding to claim 17, Chidambarrao discloses a method for improving charge mobility in a MOSFET device comprising the steps of providing a substrate comprising at least one polysilicon gate electrode; performing an ion implantation process to form dopant regions including forming an amorphous portion in the polysilicon gate electrode; and forming at least one dielectric layer comprising a selected stress level selected from the group consisting of tensile stress and compressive stress over the at least one polysilicon gate electrode (cols. 2-6).

Regarding to claim 18, the method further comprising carrying out an annealing process to recrystallize the amorphous portion and activate the dopant regions while forming a stress level the substrate.

Regarding to claim 19, the method wherein the step of forming a dielectric layer further comprises forming an underlying oxide layer (col. 4, lines 18-19).

Regarding to claim 20, the method wherein the step of forming at least one dielectric layer comprises forming a dielectric layer in tensile stress over an N-type polysilicon gate electrode and a dielectric layer in compressive stress over a P-type polysilicon gate electrode (cols. 2-6).

Regarding to claim 21, the method comprising the steps of forming a first dielectric layer comprising a first stress type selected from the group consisting of tensile and compressive stress; removing a first portion of the first dielectric layer over one of the N-type and P-type polysilicon gate electrodes; and, forming a second dielectric layer comprising a second stress type opposite from the first stress type over the first portion (cols. 2-6).

Regarding to claim 22, the method wherein the at least one dielectric layer is formed by a CVD process selected from the group consisting of LPCVD, ALCVD, and PECVD (col. 3-4).

Regarding to claim 23, the method wherein at least one dielectric layer comprises a nitride (col. 3, lines 63-65).

Regarding to claim 24, the method wherein the at least one dielectric layer is selected from the group consisting of silicon nitride and silicon oxynitride (col. 3, lines 52-67, col. 4, lines 1-8).

Regarding to claim 25, the method wherein the stress level is formed at up to about 2 Gpa (col. 3, lines 19-21).

Regarding to claim 26, the method wherein the at least one dielectric layer is formed at a thickness from about 50 Angstroms to about 1000 Angstroms (col. 4, lines 41-45).

Regarding to claim 27, the method further comprising the step of removing at least a portion of the least one dielectric layer (cols. 2-6).

Regarding to claim 28, the method further comprising the step of forming a silicide region in the uppermost portion of the polysilicon gate electrode (col. 4, lines 59-67, col. 5, lines 1-10).

Regarding to claim 29, the method wherein the step of forming the at least one dielectric layer is carried out at a temperature less than a recrystallization temperature of the amorphous portion (cols. 2-6).

Regarding to claim 30, the method wherein the step of forming at least one dielectric layer is carried out at a temperature less than about 600 degrees Celsius (col. 5, lines 33-35).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mai-Huong Tran